WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, comprising:

a first step for forming at least a region dividing groove for separating the surface of a semiconductor substrate into a first region constituting an active region of a relatively large area and a second region constituting an active region of a relatively small area;

a second step for forming an insulating film on the surface of the semiconductor substrate including the interior of the region dividing groove;

a third step for etching the insulating film using an etching mask having a lattice window pattern in such a manner that lattice openings corresponding to the lattice window pattern are formed in the first region; and

a fourth step for polishing off the insulating film remaining on the semiconductor substrate.

2. A method of fabricating a semiconductor device, comprising:

a first step for forming at least a region dividing groove for separating the surface of a semiconductor substrate into a first region constituting an active region of a relatively large area and a second region constituting an active region of a relatively small area;

a second step for forming an insulating film on the surface of the semiconductor substrate including the interior of the region dividing groove;

a third step for etching the insulating film using an etching mask having a single opening pattern and a lattice window pattern in such a manner that a single opening corresponding to the single opening pattern is formed in the first region and lattice openings corresponding to the lattice window pattern are formed in the second region; and

a fourth step for polishing off the insulating film remaining on the semiconductor substrate.

3. A method of fabricating a semiconductor device as claimed in claim 2, wherein the lattice window pattern of the etching mask has a superposed width with the active region set to a value smaller than the superposed width with the single opening pattern.

4. A method of generating a mask pattern comprising steps of:

inputting a layout pattern and dividing the layout pattern into a plurality of regions based on a predetermined rule; and

generating an inverted pattern based on a predetermined rule in a given one of a plurality of the divided regions and reshaping the inverted pattern into a lattice form.

5. A method of generating a mask pattern comprising steps of:

inputting a layout pattern and dividing the layout pattern into a plurality of regions based on a predetermined rule;

generating a first inverted pattern based on a predetermined rule in a given one of a plurality of the divided regions;

generating a second inverted pattern based on a predetermined rule in another one of a plurality of the divided regions and reshaping the inverted pattern into a lattice form; and

combining the first inverted pattern with the second inverted pattern having the lattice form.

6. A method of generating a mask pattern comprising steps of:

inputting a layout pattern and determining the amount

of a surface misalignment by simulation for the input layout pattern; and

selecting one of the mask pattern generating method as claimed in claim 4 and the mask pattern generating method as claimed in claim 5 in accordance with whether the surface misalignment determined by the simulation is minor or not.

7. A method of generating a mask pattern as claimed in claim 4, further comprising steps of:

determining the amount of a surface misalignment by simulation for the generated mask pattern; and

collating the amount of the simulated surface misalignment with an anticipated value under the predetermined rule, and in the case where the result of the collation fails to meet predetermined conditions, altering the predetermined rule and repeating each of the steps.

8. A method of generating a mask pattern as claimed in claim 7, wherein the step of determining the amount of a surface misalignment includes substeps of dividing the layout pattern into a plurality of regions, calculating the pattern density of each of the regions, and changing selected one of the superposed width with the active region and the width of the lattice form in accordance with the pattern density.

9. A method of generating a mask pattern as claimed in claim 5, further comprising steps of:

determining the amount of a surface misalignment by simulation for the generated mask pattern; and

collating the amount of the simulated surface misalignment with an anticipated value under the predetermined rule, and in the case where the result of the collation fails to meet predetermined conditions, altering the predetermined rule and repeating each of the steps.

10. A method of generating a mask pattern as claimed in claim 9, wherein the step of determining the amount of the surface misalignment includes substeps of dividing the layout pattern into a plurality of regions, calculating the pattern density of each of the regions, and changing selected one of the superposed width with the active region and the width of the lattice form in accordance with the pattern density.

11. A method of generating a mask pattern as claimed in claim 6, further comprising steps of:

determining the amount of a surface misalignment by simulation for the generated mask pattern; and

collating the amount of the simulated surface misalignment with an anticipated value under the predetermined rule, and in the case where the result of the collation fails to meet predetermined conditions, altering the predetermined rule and repeating each of the steps.

12. A method of generating a mask pattern as claimed in claim 11, wherein the step of determining the amount of a surface misalignment includes substeps of dividing the layout pattern into a plurality of regions, calculating the pattern density of each of the regions, and changing selected one of the superposed width with the active region and the width of the lattice form in accordance with the pattern density.